REMARKS

Upon entry of this amendment, claims 10-17, 56 and 57 are all the claims pending in the application. Claims 1-9 and 18-55 have been canceled by this amendment, and claims 56 and 57 have been added as new claims. Applicants note that claims 56 and 57 correspond to the elected invention.

Applicants note that a number of editorial amendments have been made to the specification for grammatical and general readability purposes. No new matter has been added.

I. Objections to the Specification

The Examiner has objected to the specification for the reasons set forth on page 2 of the Office Action. In particular, the Examiner has indicated that the features recited in claims 12 and 15 are not described in the specification.

Regarding claim 12, which recites the feature of an execution unit that "calculates (i) (a1+a1) and (a2+a2) when the first flag indicates the first status, and (ii) (a1+b1) and (a2+b2) when the first flag indicates the second status", Applicants note that this feature is described in the specification at page 35, line 20 through page 36, line 10, and is depicted in Figs. 45-47.

Regarding claim 15, which recites the feature of an execution unit that "calculates (i) (a1+a1+1) and (a2+a2+1) when the flag indicates the first status, and (ii) (a1+b1+1) and (a2+b2+1) when the flag indicates the second status", Applicants note that this feature is described in the specification at page 36, line 11 through page 37, line 3, and is depicted in Figs. 47 and 48.

In view of the foregoing, Applicants kindly request that the objections to the specification be reconsidered and withdrawn.

II. Claim Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 10-12 under 35 U.S.C. § 102(b) as being anticipated by Patterson et al. ("Computer Architecture: A Quantitative Approach").

Claim 10, as amended, recites that the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying the first register and the second register, refers to the first flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status, and (ii) on the operands held in the first register and the second register when the first flag indicates a second status. Applicants respectfully submit that Patterson does not disclose or suggest at least this feature of claim 10.

Regarding Patterson, Applicants note that this reference discloses the use of a plurality of different vector instructions (see Fig. B.3 on page B-7). For example, as shown in Fig. B.3, the instruction ADDV is utilized to perform an operation involving operands V1, V2 and V3. In particular, as shown in Fig. B.3, the associated function of ADDV is the adding of elements of V2 and V3, and placing the result of the addition in V1.

In the Office Action, the Examiner has taken the position that the second register operand of Patterson corresponds to the "flag" as recited in claim 10 (see Office Action at page 3). For example, the Examiner indicates in the Office Action that if the first and second register

operands both specify the same register, then an SIMD operation will be executed only on a single register (see Office Action at page 3).

As noted above, according to claim 10, when an instruction is present that includes operands specifying the first register and the second register, the status of a flag that is stored in a flag storage unit determines whether the SIMD operation is performed only on the operand held in the first register, or on the operands held in both the first and second registers.

Thus, according to claim 10, even though the operands specify different registers (i.e., the first register and the second register), the status of the flag can cause the SIMD operation to be performed on only the operand held in the first register.

In contrast, in Patterson, when the operands specify different registers (e.g., V2 and V3), an SIMD operation cannot be performed on an operand held only in a single register (e.g., V2). Instead, in Patterson, when the operands specify different registers (e.g., V2 and V3), the SIMD operation can only be performed on the operands held in both of the registers (i.e., V2 and V3).

According to the present invention, by providing the ability to refer to a flag in order to determine the operand(s) on which the SIMD instruction should be performed, values to be added can dynamically change depending on the status of the flag.

In view of the foregoing, Applicants respectfully submit that Patterson does not disclose, suggest or otherwise render obvious the feature of an execution unit that, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying the first register and the second register, refers to the first flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register

when the first flag stored in the flag storage unit indicates a first status, and (ii) on the operands held in the first register and the second register when the first flag indicates a second status, as recited in claim 10.

Accordingly, Applicants submit that claim 10 is patentable over Patterson, an indication of which is kindly requested. Claims 11, 12 and 56 depend from claim 10 and are therefore considered patentable at least by virtue of their dependency.

III. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 13-17 under 35 U.S.C. §103(a) as being unpatentable over Patterson et al. in view of Probin et al. ("Introduction to AltiVec Assembly Language").

Regarding claim 13, Applicants note that this claim recites that the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying the first register and the second register, refers to the flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register and rounds an operation result when the flag stored in the flag storage unit indicates a first status, and (ii) on the operands held in the first register and the second register and rounds an operation result when the flag indicates a second status.

Thus, similar to the discussion above, according to claim 13, when an instruction is present that includes operands specifying the first register and the second register, the status of a flag that is stored in a flag storage unit determines whether the SIMD operation is performed only on the operand held in the first register, or on the operands held in both the first and second registers.

Therefore, as is evident from claim 13, even though the operands specify different registers (i.e., the first register and the second register), the status of the flag can cause the SIMD operation to be performed only on the operand held in the first register. For at least similar reasons as discussed above, Applicants respectfully submit that Patterson does not disclose or suggest such a feature. Further, Applicants respectfully submit that Probin does not cure this deficiency of Patterson.

In view of the foregoing, Applicants respectfully submit that the combination of Patterson and Probin does not disclose, suggest or otherwise render obvious at least the above-noted feature recited in claim 13. Accordingly, Applicants submit that claim 13 is patentable over the cited prior art, an indication of which is kindly requested. Claims 14, 15 and 57 depend from claim 13 and are therefore considered patentable at least by virtue of their dependency.

Regarding claims 16 and 17, Applicants note that both of these claims depend from claim 10. Applicants submit that Probin fails to cure the deficiencies of Patterson, as discussed above, with respect to claim 10. Accordingly, Applicants submit that claims 16 and 17 are patentable at least by virtue of their dependency.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited.

If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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